

FEATURES

- STHC (Super Twisted High Contrast) Yellow Green Transmissive Type
- Low Power Consumption
- Thin, Lightweight Design Permits Easy Installation in a Variety of Equipment
- General-Purpose CMOS:
 - The Unit can be Easily Interfaced to a Microcomputer with Common 4-Bit and 8-Bit Parallel Inputs and Outputs
- Built-in Character Generator ROM, RAM, and Display Data RAM:
 - Character Generator ROM – 160 Different 5×7 Dot Matrix Character Patterns
 - Character Generator RAM – Eight Different, User-Programmed 5×7 Dot Matrix Patterns (Write Capability by Program)
 - Display Data RAM – 80×8 bits

- Extensive Instruction Set:
 - Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Character Blink, Cursor Shift, and Display Shift
- Internal Automatic Reset Circuit at Power-On
- Operates From a Single 5 V Power Supply and Incorporates an LCD Panel Which Provides a Highly Stable Display Over a Wide Range of Temperatures

DESCRIPTION

The SHARP LM40X21A Dot Matrix LCD Unit consists of a combination of a 5×7 dot 40-character 2-line dot matrix LCD panel, LCD driver, and controller LSI and yellow green backlight LED mounted on a single printed circuit board. Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the unit is capable of efficiently displaying the desired characters under microcomputer control. LCD is positive type.

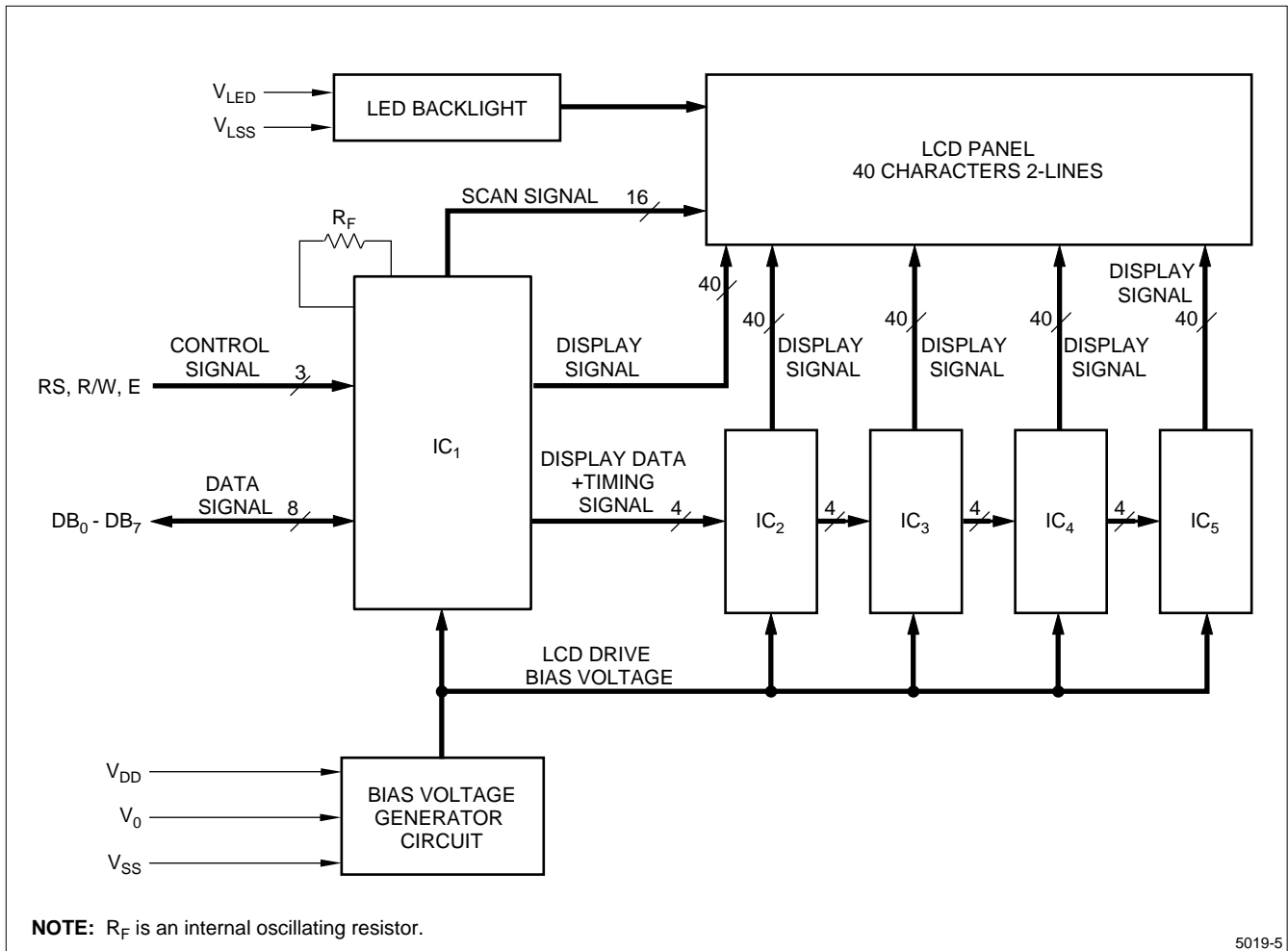


Figure 1. LM40X21A Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT	NOTE
Outline Dimensions	182 (W) × 33.5 (H) × 16 max (D)	mm	–
Active Area	154.4 (W) × 15.8 (H)	mm	–
Display Format	40 characters × 2 lines	–	–
Character Format	5 × 7 dots, with cursor	–	–
Character Size	3.2 (W) × 4.85 (H) (5 × 7 dots)	mm	–
Dot Size	0.6 (W) × 0.65 (H)	mm	–
Dot Spacing	0.05	mm	–
Character Color	Dark blue	–	1
Backlight Color	Yellow Green	–	–
Weight	Approximately 90	g	–

NOTE:

1. Due to the characteristics of the LC material, the color varies with the environmental temperature.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
$V_{DD} - V_{SS}$	Supply Voltage (Logic)	-0.3	+6.5	V	–
$V_O - V_{SS}$	Supply Voltage (LCD Drive)	0	+6.5	V	$V_{DD} > V_O$
I_{LED}	Supply Current (Backlight LED)	–	400	mA	$t_A = 25^\circ\text{C}$
V_{IN}	Input Voltage	-0.3	$V_{DD} + 0.3$	V	–
T_{stg}	Storage Temperature	-25	+70	$^\circ\text{C}$	–
T_{opr}	Operating Temperature	0	+50	$^\circ\text{C}$	–
$V_{LED} - V_{LSS}$	Reverse Voltage (Backlight LED)	-5	–	V	–

ELECTRICAL CHARACTERISTICS ($t_A = 25^\circ\text{C}$)

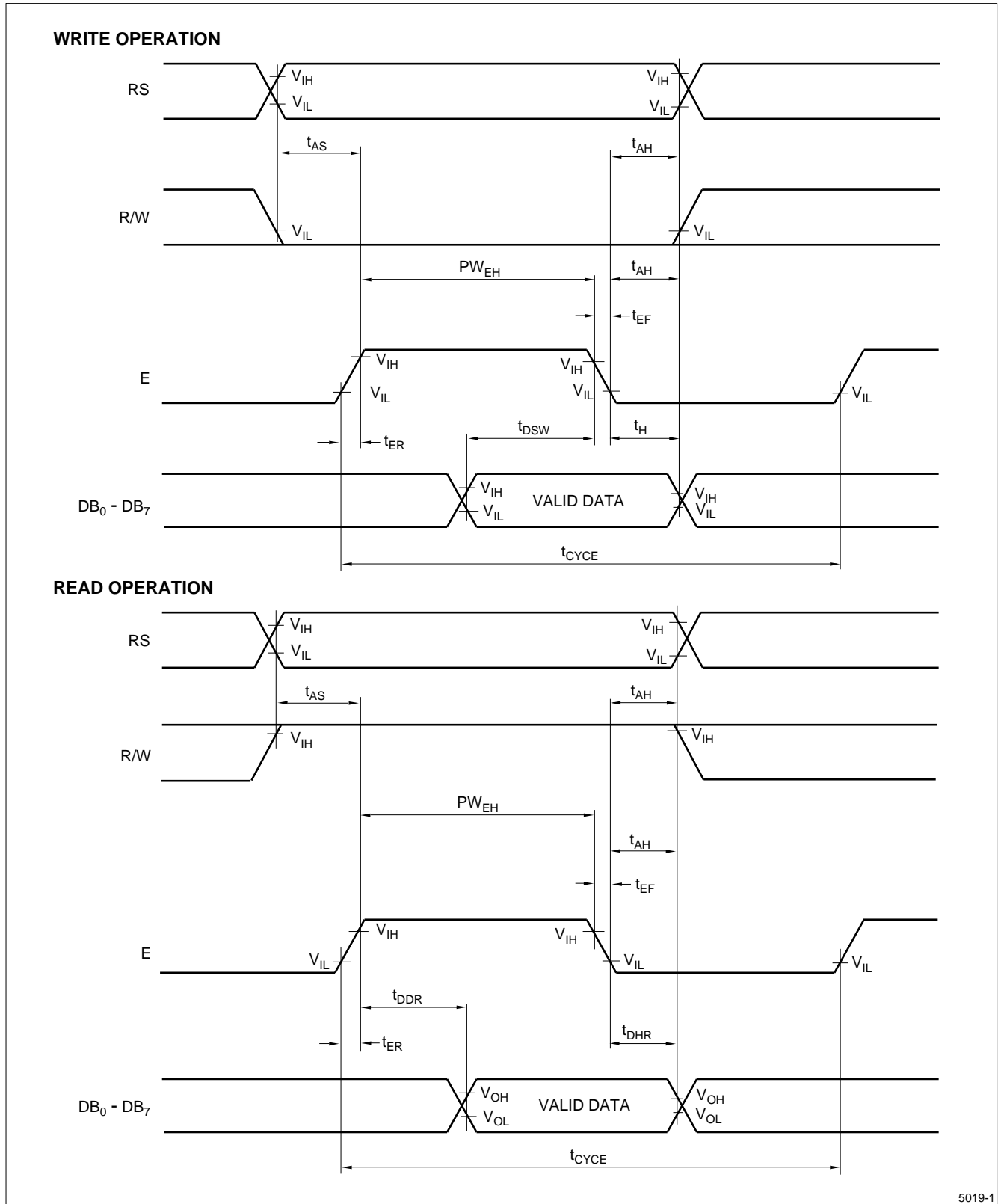
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE
$V_{DD} - V_{SS}$	Supply Voltage (Logic)		4.75	5.0	5.25	V	–
$V_O - V_{SS}$	Supply Voltage (LCD Drive)		–	0.65	–	V	$V_{DD} = 5.0\text{ V}$ Note 1
V_{IL}	Input Voltage	'L'	–0.3	–	0.6	V	–
V_{IH}		'H'	2.2	–	V_{DD}	V	–
V_{OL}	Output Voltage	'L'	–	–	0.4	V	$I_{OL} = 1.2\text{ mA}$
V_{OH}		'H'	2.4	–	–	V	$I_{OH} = -0.205\text{ mA}$
I_{IL}	Input Leakage Current		–	–	1	μA	–
f_{OSC}	Internal Oscillating Frequency		–	160	–	kHz	–
I_{DD}	Supply Current		–	2.4	3.5	mA	$V_{DD} = 5.0\text{ V}$ $V_O = 0\text{ V}$
I_{LED}			–	300	400	mA	$V_{LED} - V_{LSS} = 5.0\text{ V}$
P_D	Power Dissipation		–	1512	2017.5	mW	$V_{DD} = 5.0\text{ V}, V_O = 0\text{ V}$ $V_{LED} - V_{LSS} = 5.0\text{ V}$
$V_{LED} - V_{LSS}$	Supply Voltage (Backlight LED)		4.75	5.0	5.25	V	–

NOTE:

1. When more than 60 minutes have elapsed since backlighting began.

INTERFACE TIMING ($V_{DD} = 5.0\text{ V} \pm 5\%$, $t_A = 0\text{ to }50^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{CYCE}	Enable Cycle Time	1000	–	–	ns
PW_{EH}	Enable Pulse Width	450	–	–	ns
t_{ER}, t_{EF}	Enable Rise/Fall Time	–	–	25	ns
t_{AS}	RS, R/W Setup Time	140	–	–	ns
t_{AH}	Address Hold Time	10	–	–	ns
t_{DSW}	Data Setup Time	195	–	–	ns
t_{DDR}	Data Delay Time	–	–	320	ns
t_H	Data Hold Time (Write)	10	–	–	ns
t_{DHR}	Data Hold Time (Read)	20	–	–	ns



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Figure 2. Interface Timing Chart

PIN CONNECTIONS

PIN NUMBER	SYMBOL	DESCRIPTION	CONNECTION
1	V _{SS}	Ground Potential	GND: 0 V
2	V _{DD}	Power Supply (Logic)	+5 V Power Supply
3	V _O	Contrast Adjustment Voltage	Adjust the contrast by supplying voltage from 0 V to 5 V
4	RS	Register Select Pin	Control signal inputs
5	R/W	Read/Write Select Pin	
6	E	Enable Pin	
7	DB ₀	Code I/O Data LSB	<ul style="list-style-type: none"> • Data bus signals • DB₇ may also be used to check the busy flag • DB₀ to DB₃ are not used when interfacing with a 4-bit microprocessor
8	DB ₁	Code I/O Data 2nd Bit	
9	DB ₂	Code I/O Data 3rd Bit	
10	DB ₃	Code I/O Data 4th Bit	
11	DB ₄	Code I/O Data 5th Bit	
12	DB ₅	Code I/O Data 6th Bit	
13	DB ₆	Code I/O Data 7th Bit	
14	DB ₇	Code I/O Data MSB	
15	V _{LED}	Power Supply (+)	5 V power supply between V _{LED} and V _{LSS}
16	V _{LSS}	Power Supply (-)	

OPTICAL CHARACTERISTICS ($V_{DD} - V_O = 4.0 \text{ V}$, $t_A = 25^\circ\text{C}$) (When Backlight LED is in the OFF State)

The table below shows the optical characteristics when LCD drive voltage is adjusted to the maximum contrast in $\theta = 0^\circ$.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
$\theta_2 - \theta_1$	Viewing Angle Range	$\phi = 0^\circ$ $C_0 \geq 2.0$	60	—	—	degrees	1
θ_1			—	—	-25		
θ_2		$\theta_1 < \theta_2$ $C_0 = 2.0$	25	—	—		
$\theta_2 - \theta_1$			$\phi = 45^\circ$ 315° $\theta_1 < \theta_2$	60	—		
θ_1		$C_0 = 2.0$		—	—		
θ_2			25	—	—		
C_0	Contrast Ratio	$\theta = 0^\circ, \phi = 0^\circ$	5.0	8.0	—	—	2
t_R	Response Speed – Rise	$\theta = 0^\circ, \phi = 0^\circ$	—	150	250	ms	3
t_D	Response Speed – Decay	$\theta = 0^\circ, \phi = 0^\circ$	—	150	250	ms	

NOTES:

- The viewing angle range is defined as shown in Figure 3.
- Contrast ratio is defined as follows:
When input signal is applied to the unit to select (turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Figure 4.

$$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non-select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$
- When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Figure 4. The response characteristics of the photodetector output are measured as shown in Figure 5.

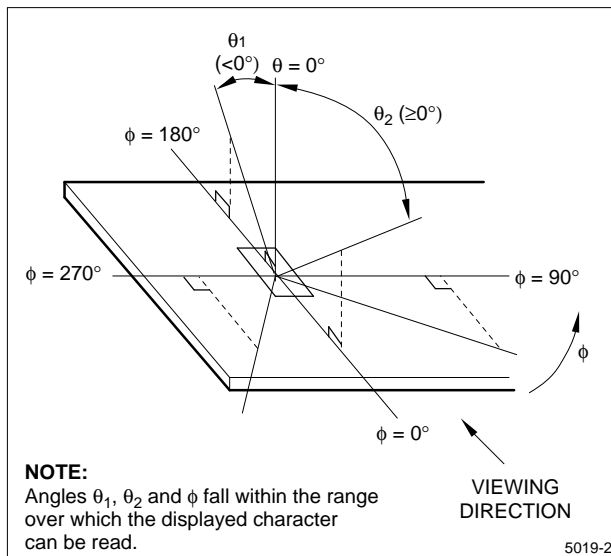


Figure 3. Definition of Viewing Angle

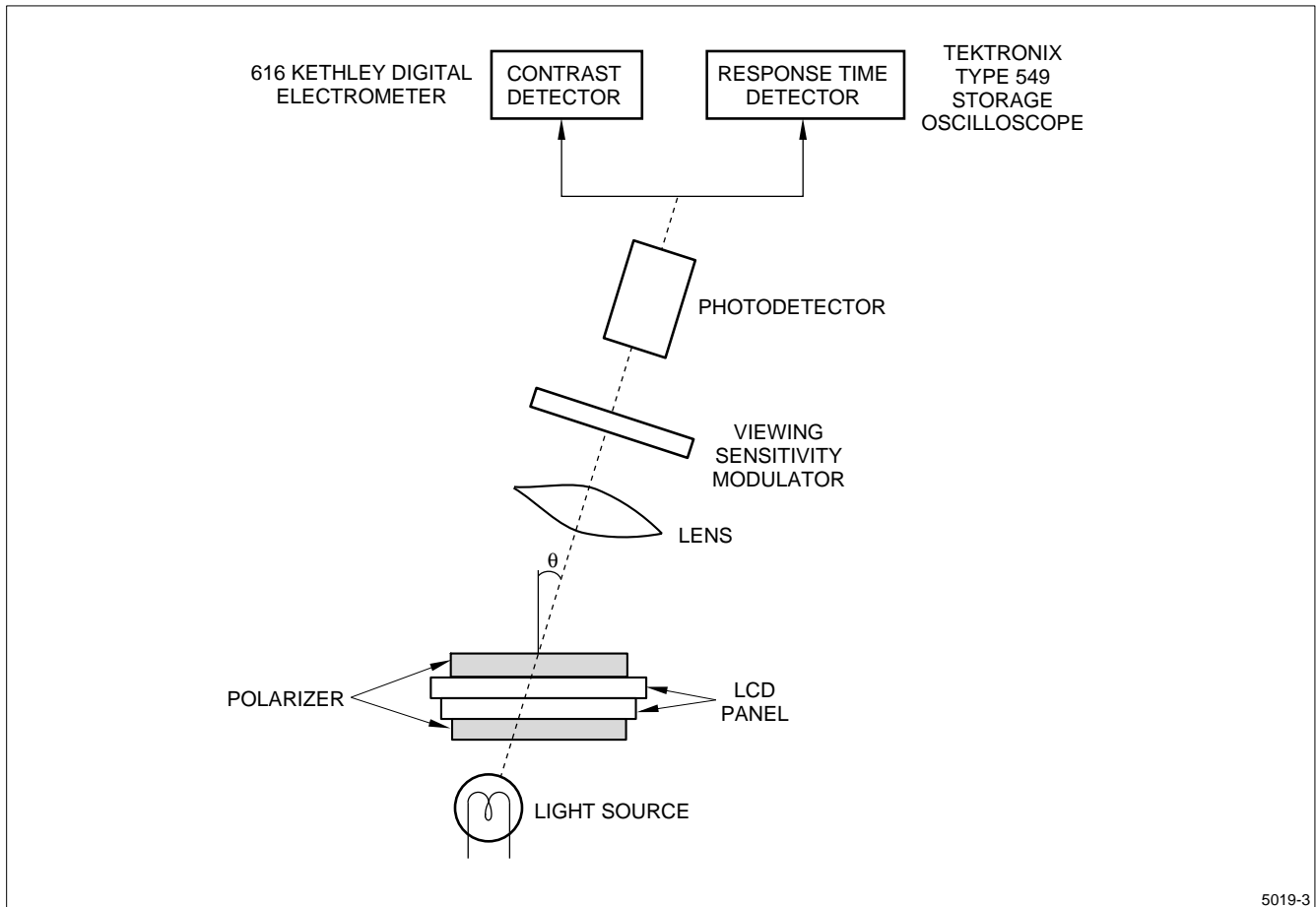


Figure 4. Optical Characteristics Test Method

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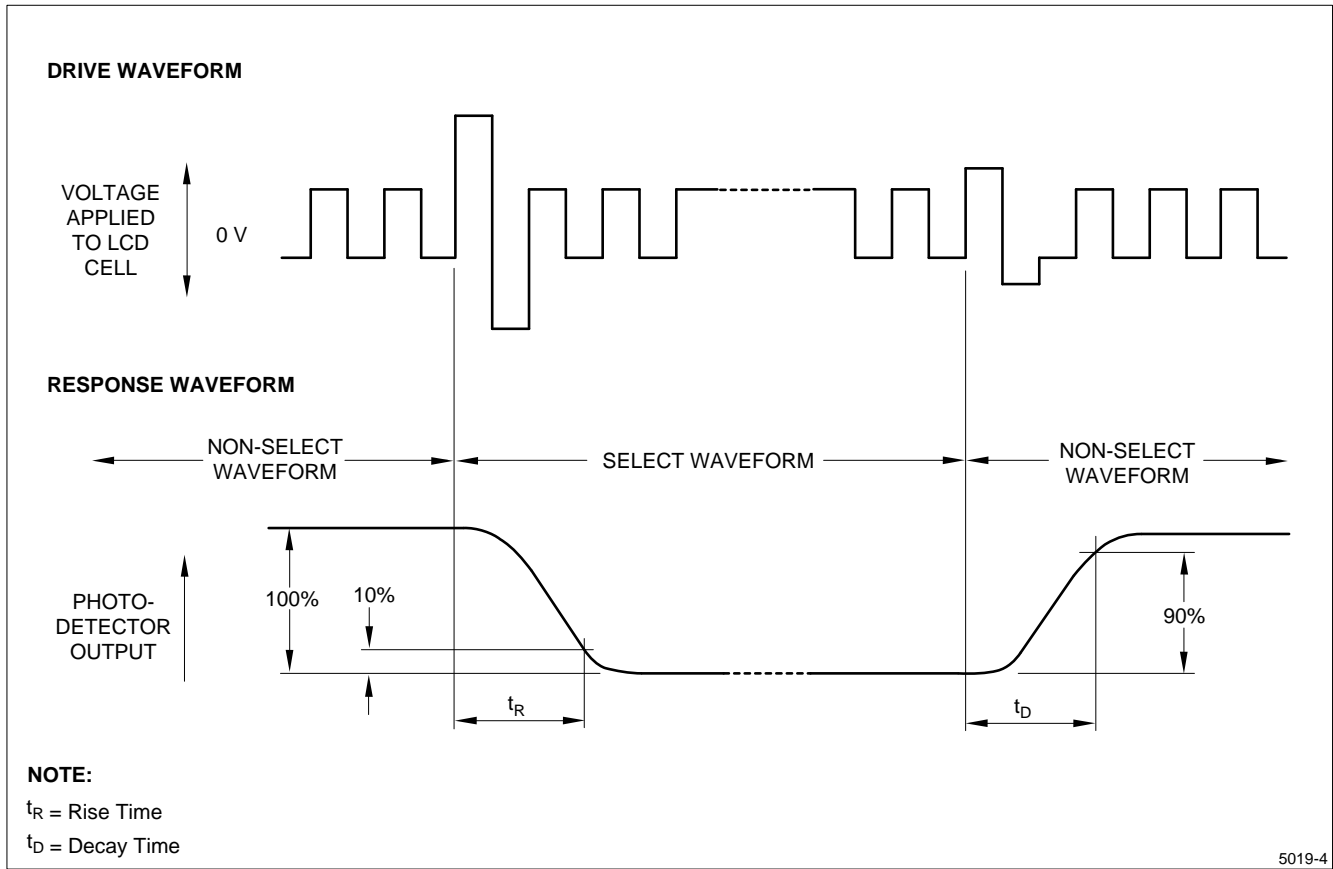


Figure 5. Definition of Response Time

CHARACTERISTICS OF BACKLIGHT LED ($t_A = 25^\circ\text{C}$, $V_{\text{LED}} - V_{\text{LSS}} = 5.0\text{ V}$)

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Luminance	7	22	–	cd/m ²	1
Peak emission wavelength	–	565	–	nm	–
Spectrum radiation bandwidth	–	30	–	nm	–

NOTE:

1. Center of the unit with LED backlight lit.

PIN DESCRIPTION**V_{DD} and V_{SS} Pins**

V_{DD} and V_{SS} pins are for the power supply. V_{SS} pin is grounded, and V_{DD} pin is supplied with +5 V. Each voltage necessary to drive LCD is generated in the unit.

RS Pin

The controller LSI contains two 8-bit registers: instructions register (IR) and data register (DR). RS pin selects these registers.

IR serves to store instruction codes for display clear, shift, etc. and address information for display data RAM (DD RAM), character generator RAM (CG RAM); DR serves to temporarily store data to be written into DD RAM and CG RAM.

'0': Instruction register (Write)
Busy flag register; address counter (Read)

'1': Data register (Read/Write)

R/W Pin

Read or write selection signal pin.

'0': Write

'1': Read

E Pin

Data read or write operation enable signal pin.

DB₀ to DB₇ Pins

Tri-state bidirectional data bus pins. The bus allows data to be transmitted to or received from the external circuit. DB₇ serves also as busy flag output. When the unit is interfaced to a microcomputer with 4-bit parallel outputs, DB₀ to DB₃ pins are not used.

V₀ Pin

Viewing angle is varied and contrast is adjusted by changing input voltage between +5 V to 0 V by applying bias voltage to the LCD driver.

V_{LED} and V_{LSS}

Power supply for LED backlight. (By changing the supply voltage, backlight luminance can be adjusted). V_{LED} is plus and V_{LSS} is minus.

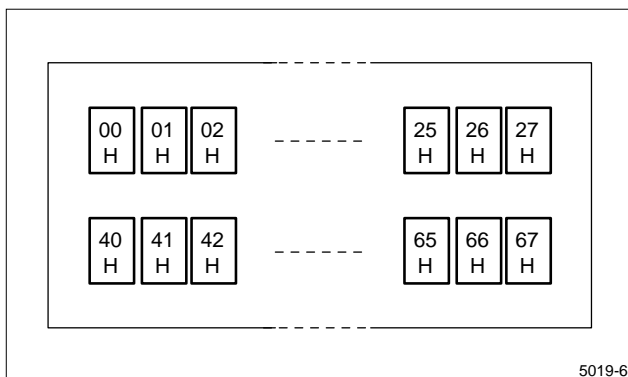
INSTRUCTION SET

INSTRUCTION	CODES										DESCRIPTION
	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀	
Display Clear	0	0	0	0	0	0	0	0	0	1	Clears entire display area, restores display from shift, and loads address counter with DD RAM address 00H.
Cursor Home	0	0	0	0	0	0	0	0	1	*	Restores display from shift and loads address counter with DD RAM address 00H.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specifies cursor advance direction and displays shift mode. This operation takes place after each data transfer.
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specifies activation of display (D), cursor (C), and blinking of character at cursor position (B).
Cursor/ Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shifts display or moves cursor.
Function Set	0	0	0	0	1	DL	1	0	*	*	Sets interface data length (DL).
CG RAM Address Set	0	0	0	1	ACG					Loads the address counter with CG RAM address. Subsequent data is CG RAM data.	
DD RAM Address Set	0	0	1	ADD					Loads the address counter with a DD RAM address. Subsequent data is DD RAM DATA.		
Busy Flag/ Address Counter Read	0	1	BF	AC					Reads out busy flag (BF) and contents of address counter (AC).		
CG RAM/ DD RAM Data Write	1	0	Write data					Writes data into DD RAM or CG RAM.			
CG RAM/ DD RAM Data Read	1	1	Read data					Reads data from DD RAM or CG RAM.			

NOTES:

I/D = 1: Increment
 S = 1: Display shift
 D = 1: Display ON
 C = 1: Cursor ON
 B = 1: Character at cursor position blinks
 I/D = 0: Decrement
 S = 0: Display freeze
 D = 0: Display OFF
 C = 0: Cursor OFF

B = 0: Character at cursor position unblinks
 S/C = 1: Display shift
 R/L = 1: Right shift
 DL = 1: 8 bits
 BF = 1: During internal operation
 S/C = 0: Internal cursor shift
 R/L = 0: Left shift
 DL = 0: 4 bits
 BF = 0: End of internal operation



**Figure 6. Display Address
 (When the Display is Not Shifted)**

HIGH-ORDER LOW-ORDER 4 BIT	HIGH-ORDER												
	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	a	P	`	P	-	9	E	e	*	
xxxx0001	(2)	!	1	A	Q	a	9	7	7	4	ä	*	
xxxx0010	(3)	"	2	B	R	b	r	"	4	W	×	*	0
xxxx0011	(4)	#	3	C	S	c	s	,	0	T	E	e	∞
xxxx0100	(5)	\$	4	D	T	d	t	,	I	T	†	*	Ω
xxx0101	(6)	%	5	E	U	e	u	.	+	+	1	0	Ü
xxx0110	(7)	&	6	F	V	f	v	7	0	二	ヨ	*	Σ
xxxx0111	(8)	'	7	G	W	g	w	7	+	又	う	*	π
xxxx1000	(1)	(8	H	X	h	x	4	0	*	リ	5	又
xxxx1001	(2))	9	I	Y	i	y	9	7	リ	ル	"	*
xxxx1010	(3)	*	:	J	Z	j	z	±	コ	ハ	ル	*	7
xxxx1011	(4)	+	;	K	L	k	l	(7	ヒ	ロ	*	ア
xxxx1100	(5)	,	<	L	*	l	l	7	ヨ	フ	ワ	0	ア
xxxx1101	(6)	-	=	M	I	m	i)	ユ	ズ	ハ	ト	÷
xxxx1110	(7)	.	>	N	^	n	→	ヨ	E	ホ	ハ	ハ	
xxxx1111	(8)	/	?	O	_	o	←	ウ	リ	マ	°	ö	*

NOTES:

1. CG RAM is character generator RAM in which user-definable character patterns are stored.
2. X mark: prohibition of input.

Figure 7. Input Code vs. Character Pattern

OUTLINE DIMENSIONS

